# 6.004 Tutorial Problems

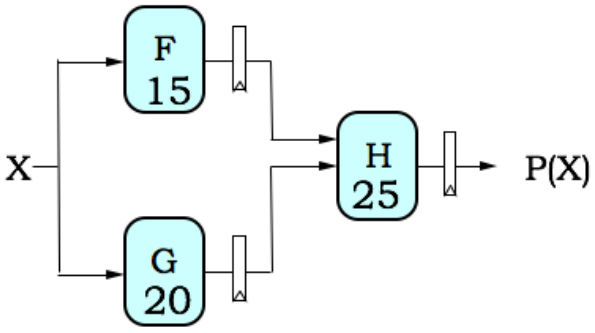
## L12 – Introduction to Pipelining

**Latency**: the delay from when an input is established until the output associated with the input becomes valid.

- Combinational circuits: $L = t_{PD}$
- K-pipeline: $L = K*t_{CLK}$

**Throughput**: the rate at which inputs or outputs are processed.

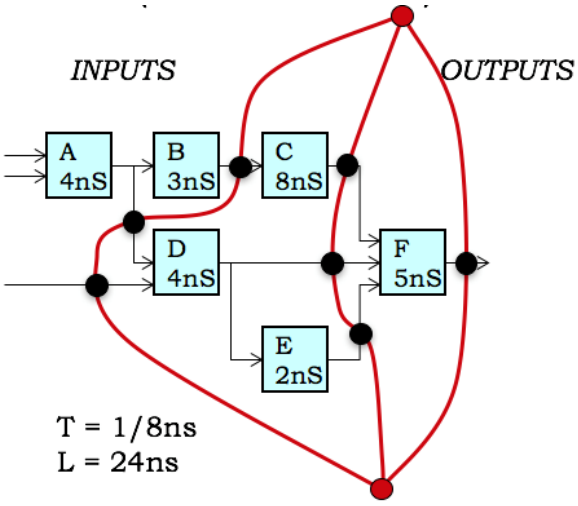
- Combinational circuits: $T = 1/L$
- K-pipeline: $T = 1/t_{CLK}$

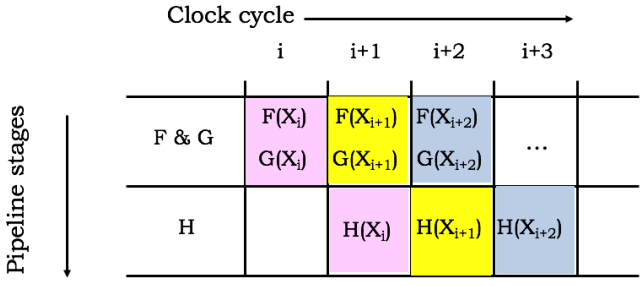



Unpipelined:
L = 45ns, T = 1/L = 1/(45ns)
2-stage pipeline [$t_{CLK}$=25ns]:
L = 2*25 = 50 ns, T = 1/(25ns)

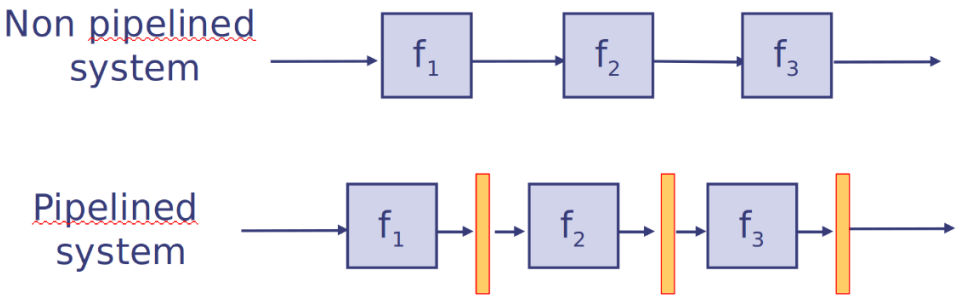
**Pipelining methodology**:

- Form 1-pipeline by adding registers to all outputs
- To add a pipeline stage, draw contour across all paths from inputs to outputs such that it doesn't cross other contours and all input-output paths cross the contour in the same direction. This ensures the pipeline is well-formed (same # of registers on all input-output paths). A K-pipeline has K registers on all input-output paths.
- Contours must take into account pipelined components.



Pipelining trades improved Clock Period and Throughput for worse Latency. Consider the example shown below:




Suppose the latency of

- $f_1$ and $f_3$ is 5ns
- $f_2$ is 6ns
- register is 0ns

| | Non pipelined | Pipelined |
|---|---|---|
| Clock period (ns) | 5+6+5=16 | 6 |
| Throughput (1/ns) | 1/16 | 1/6 |
| Latency (ns) | 16 | 3*6 = 18 |

**Problem 1.** ★

A simple combinational circuit is to be pipelined for **maximum throughput using a minimal number of registers**. For each of the questions below, please create a valid K-stage pipeline. **Show your pipelining contours** and place large black circles (●) on the signal arrows to **indicate the placement of ideal pipeline registers** (tPD=0, tSETUP=0). Give the latency and throughput for each design. Remember that our convention is to place a pipeline register on each output.

(A) (1 point). Show the maximum-throughput 1-stage pipeline.

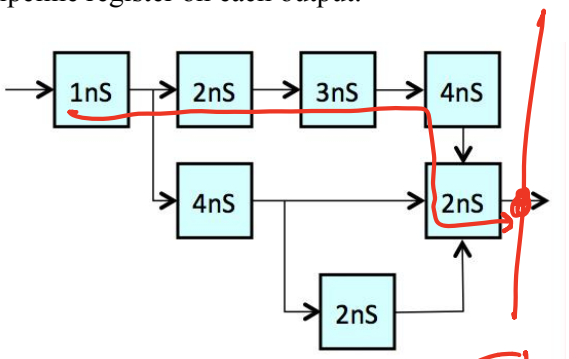
Throughput = 1 / clock period

Units: $[ns^{-1}] = \frac{1}{[ns]}$

**Latency (ns):** 12ns

**Throughput (ns-1):** 1/12

(1+2+3+4+2) ns = 12ns




(B) (2 points). Show the maximum-throughput 2-stage pipeline using a minimal number of registers.

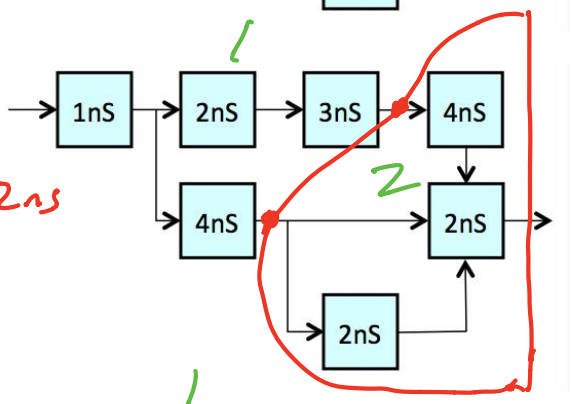
**Pipelining methodology**:
- Form 1-pipeline by adding registers to all outputs
- To add a pipeline stage, draw contour across all paths from inputs to outputs such that it doesn't cross other contours and all input-output paths cross the contour in the same direction. This ensures the pipeline is well-formed (same # of registers on all input-output paths). A K-pipeline has K registers on all input-output paths.
- Contours must take into account pipelined components.

**Latency (ns):** 2x6=12ns

**Throughput (ns-1):** 1/6

1+2+3=6 ns

4ns+2ns=6ns




(C) (2 points). Show the maximum-throughput 3-stage pipeline using a minimal number of registers.

Step 1: find the longest path

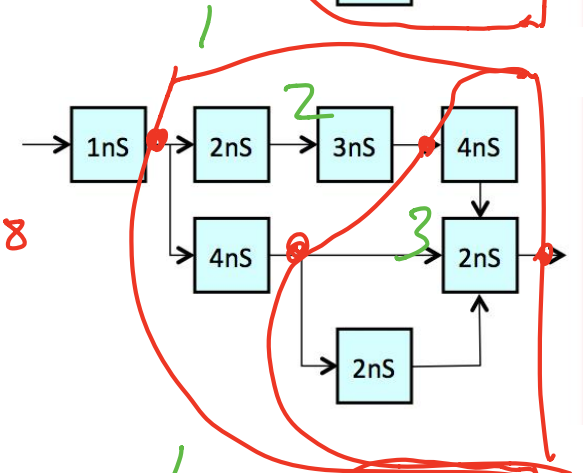
Step 2: chop of the closest subpath

Step 3: Chop off other parts

**Latency (ns):** 3x6=18

**Throughput (ns-1):** 1/6

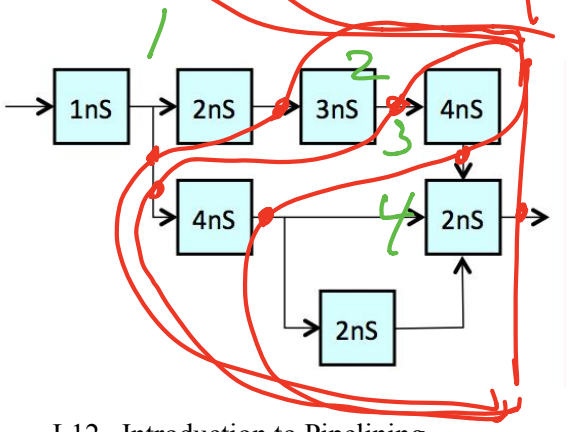
Not enough to see benefit




(D) (2 points). Show the maximum-throughput 4-stage pipeline using a minimal number of registers.

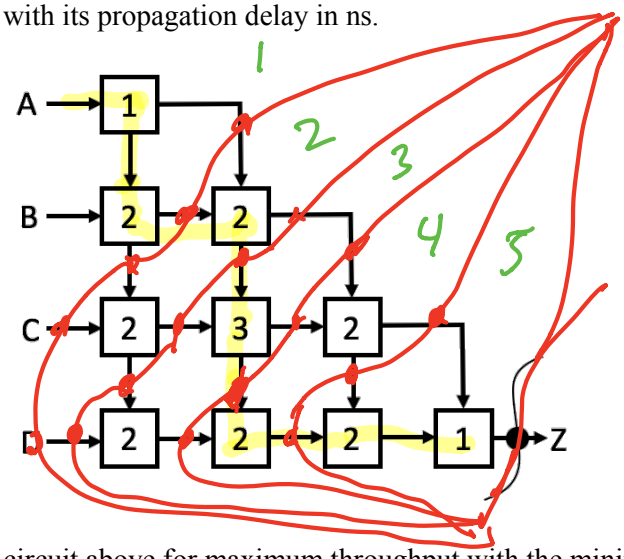
**Latency (ns):** 4x4=16

**Throughput (ns-1):** 1/4



**Problem 2.**

The following 1-stage pipelined circuit computes Z from the four inputs A, B, C, and D. Each component is annotated with its propagation delay in ns.




5-pipelined

(A) Please pipeline the circuit above for maximum throughput with the minimum possible latency using ideal pipeline registers ($t_{PD}$ = 0, $t_{SETUP}$ = 0). Show the location of pipeline registers in the diagram above using filled-in circles, like the one shown on the Z output. Please give the latency and throughput of the resulting pipelined circuit.

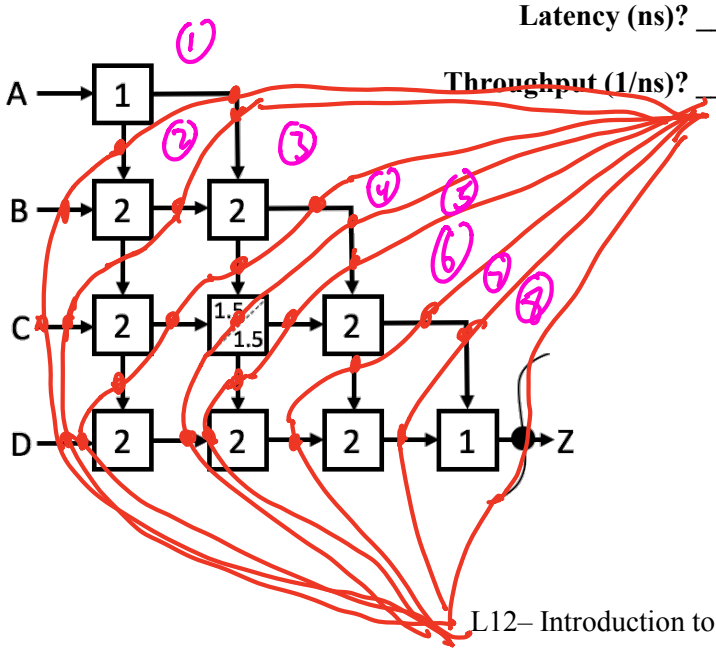
**Latency (ns)?** 5 x 3 = 15ns

**Throughput (1/ns)?** 1/3

(B) Now suppose the "3" component is replaced by a 2-stage pipelined component with a minimum $t_{CLK}$ of 1.5ns. Again, please pipeline the circuit below for maximum throughput with the minimum possible latency using ideal pipeline registers. Show the location of pipeline registers in the diagram below using filled-in circles, like the one shown on the Z output. Please give the latency and throughput of the resulting pipelined circuit.

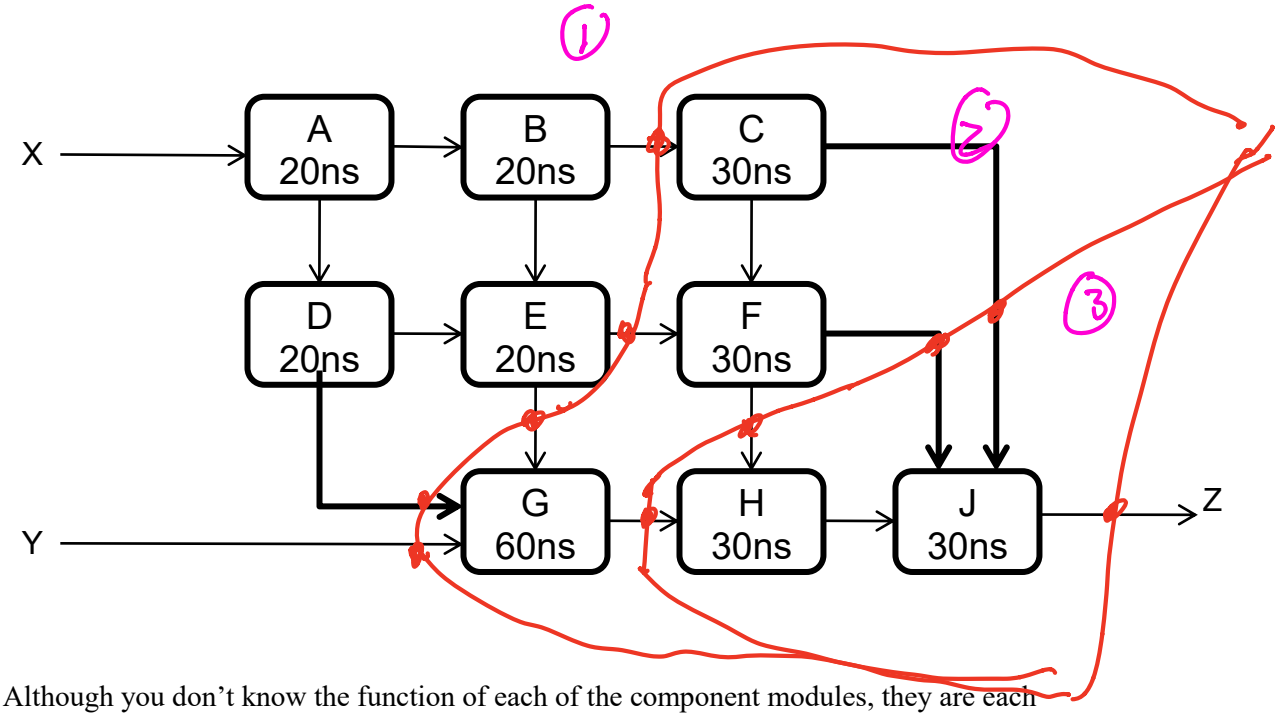
**Latency (ns)?** 8 x 2ns = 16ns

**Throughput (1/ns)?** 1/2



**Problem 3.**

An unidentified government agency has a design for a combinational device depicted below:




Although you don't know the function of each of the component modules, they are each combinational and marked with their respective propagation delays. You have been hired to analyze and improve the performance of this device.

(A) (1 Point) What are the throughput and latency for the unpipelined combinational device?

3 x 60 ns = 180 ns

**Latency:** 180 **ns; Throughput:** 1/180 **ns$^{-1}$**

(B) (4 Points) Show how to pipeline the above circuit for maximum throughput, by marking locations in the diagram where registers are to be inserted. **Use a minimum number of registers, but be sure to include one on the output**. Assume that the registers have 0 $t_{PD}$ and $t_{SETUP}$.

10

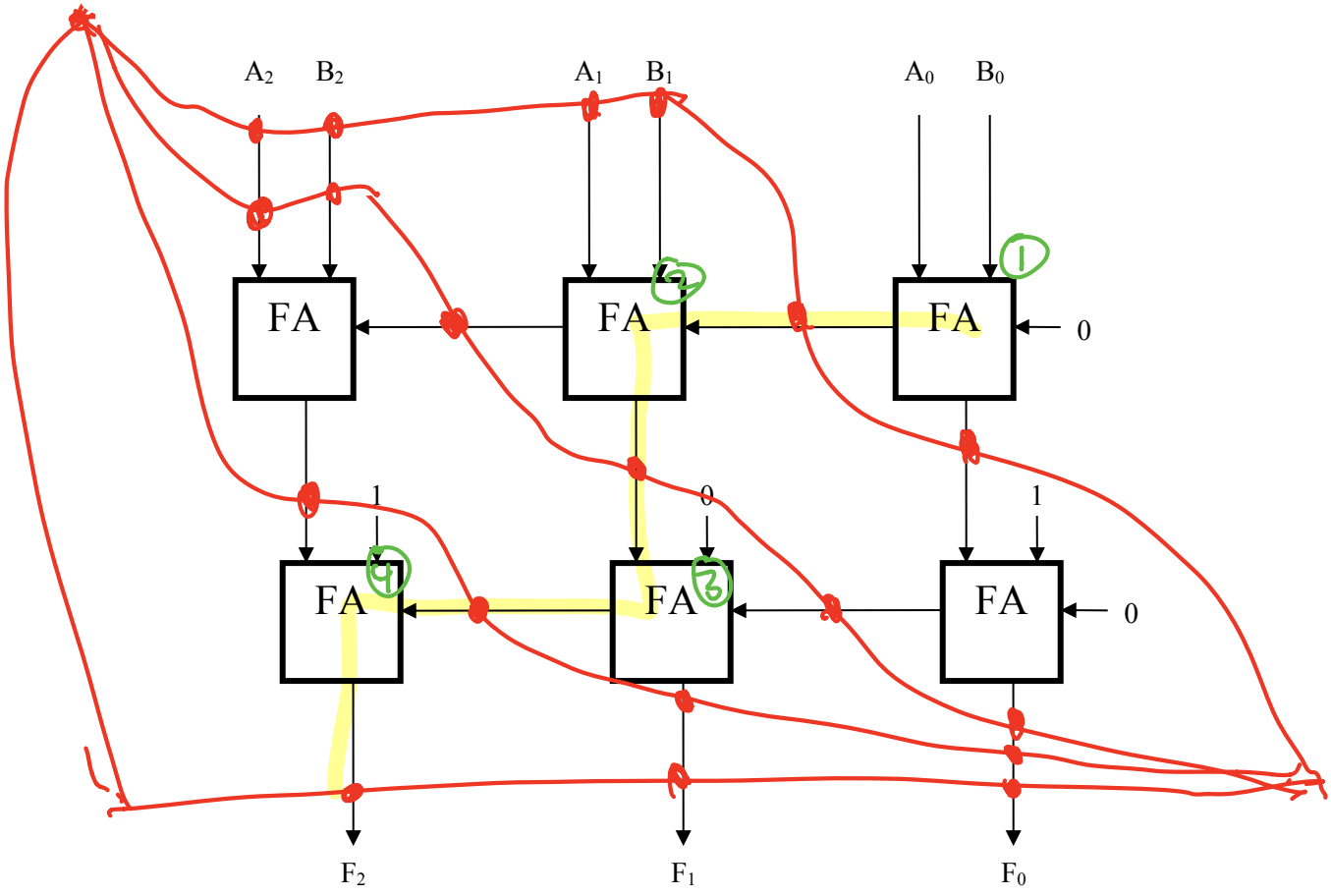
**(mark register locations in diagram above)**

(C) (1 Point) What are the latency and throughput of your pipelined circuit?

**Latency:** 180 **ns; Throughput:** 1/60 **ns$^{-1}$**

**Problem 4.** ★

The following circuit uses six full adder modules (as you've seen in lecture and lab) arranged in a combinational circuit that computes a 3-bit value **F=A+B+5** for 3-bit inputs **A** and **B**:




The full adders have a $t_{PD}$ of 6ns.

(A) Give the latency and throughput of the combinational circuit.

(1 pipeline) 6 × 4 = 24ns **Latency:** 24 **ns; Throughput:** 1/24

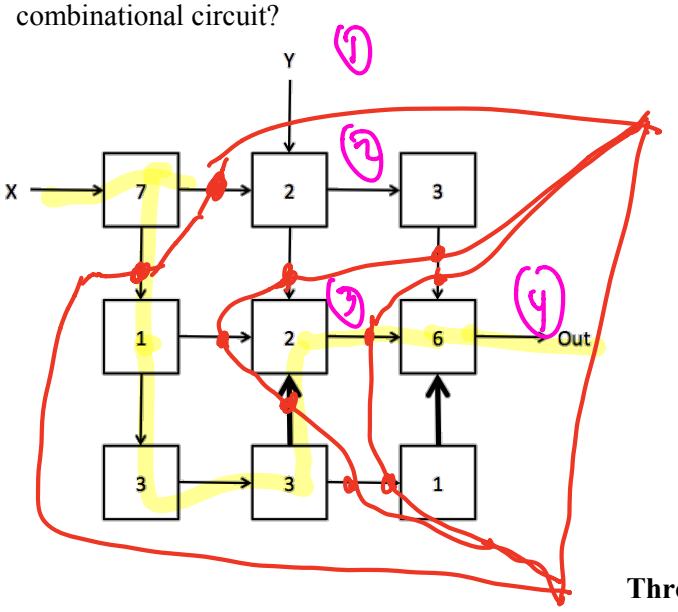
(B) Indicate, on the above diagram, appropriate locations to place ideal (zero-delay) registers to pipeline the circuit for *maximum throughput* using a *minimum number of registers*. Be sure to include a register on each output. 19 **(mark circuit above)**

(C) Give the latency and throughput of your pipelined circuit.

4 × 6 = 24ns **Latency:** 24 **ns; Throughput:** 1/6

**Problem 5.** ★

(A) You are provided with the circuit shown below. Each box represents some combinational logic. The number in each box is the $t_{PD}$ of that combinational logic. The circuit has two inputs, X and Y, and one output Out. Pay close attention to the direction of the arrows especially the arrows shown in **bold**. What is the latency and throughput of this combinational circuit?




This is the most optimal

7+1+3+3+2+6 = 22

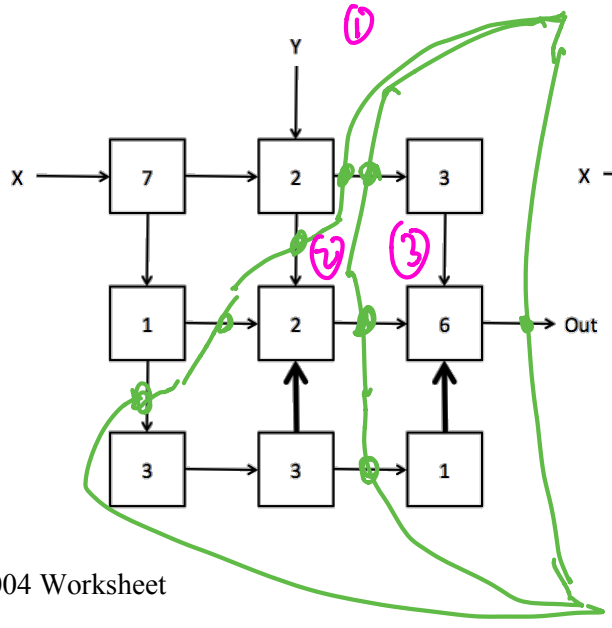
**Latency (ns):** 22

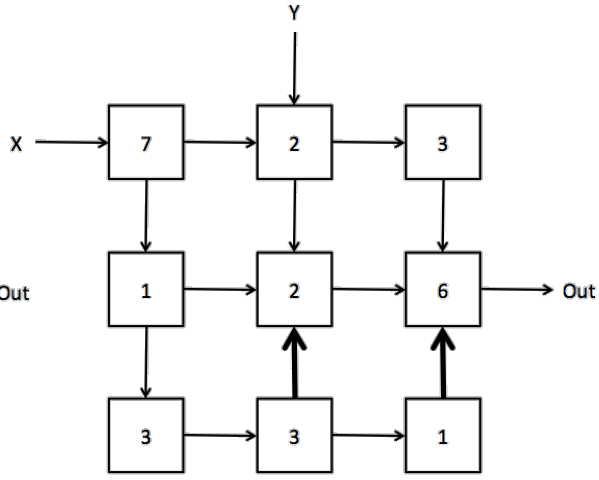
**Throughput (1/ns):** 1/22

(B) Draw contours through the circuit above to produce a valid pipelined circuit **whose $t_{CLK}$ = 9ns with minimum latency**. Extra copies of the diagram are included below. Please use a large dot to **indicate the location of each pipeline register**. Assume that you have ideal pipeline registers ($t_{PD}=t_{CD}=t_{Setup}=t_{Hold}=0$ ns). Pay close attention to the direction of each arrow to ensure that you produce a valid pipeline. What is the latency and throughput of this pipelined circuit?

**Latency (ns):** 9 x 3 = 27 ns

**Throughput (1/ns):** 1/9

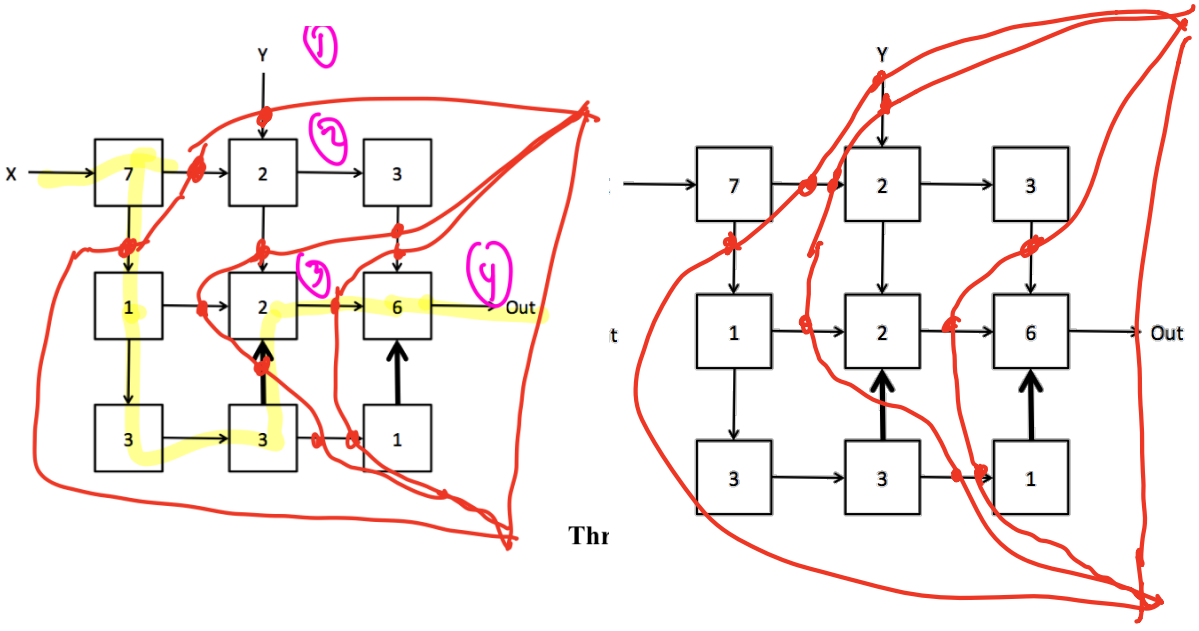


(C) You are now asked to consider the performance of this circuit using different clock periods while achieving the minimum latency. For each suggested $t_{CLK}$, specify whether or not you can create a **valid** pipelined circuit using that clock period. If you can, then provide the latency and throughput of the resulting circuit and specify the number of registers at each input. If it results in an invalid pipeline, enter NA for the rest of the row.

Extra copies of the circuit diagram are provided below.

| $t_{CLK}$ | Valid/Invalid | Latency (ns) | Throughput (1/ns) | Pipeline registers at input X | Pipeline registers at input Y |
|---|---|---|---|---|---|
| 6 ns | invalid | | | | |
| 7 ns | valid | 28 ns | 1/7 | 0 | 1 or 2 |



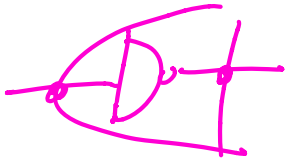

**Problem 6.**

A complex combinational circuit is constructed entirely from 2-input NAND gates having a propagation delay of 1 ns. If this circuit is pipelined for maximal throughput by adding (non-ideal) registers whose setup time and propagation delay are each 1 ns, what is the throughput of the resulting pipeline? Enter a number, a formula, or "CAN'T TELL".

**Throughput ($ns^{-1}$):** 1/3

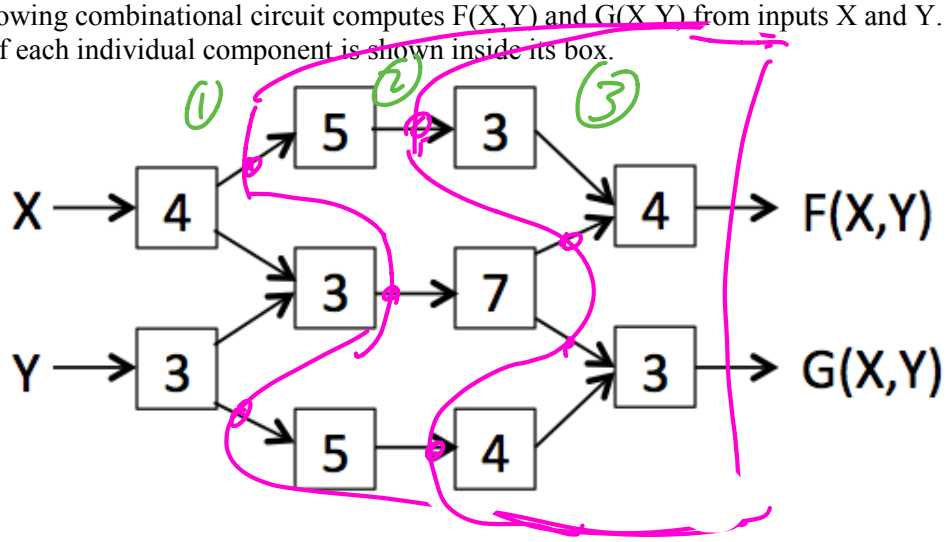
$t_{CLK} \geq t_{PD,R} + t_{PD,NAND} + t_{setup,R}$

$\Rightarrow t_{CLK} \geq 1 + 1 + 1 = 3\ ns$



**Problem 7.**

The following combinational circuit computes F(X,Y) and G(X,Y) from inputs X and Y. The $t_{PD}$ (in ns) of each individual component is shown inside its box.

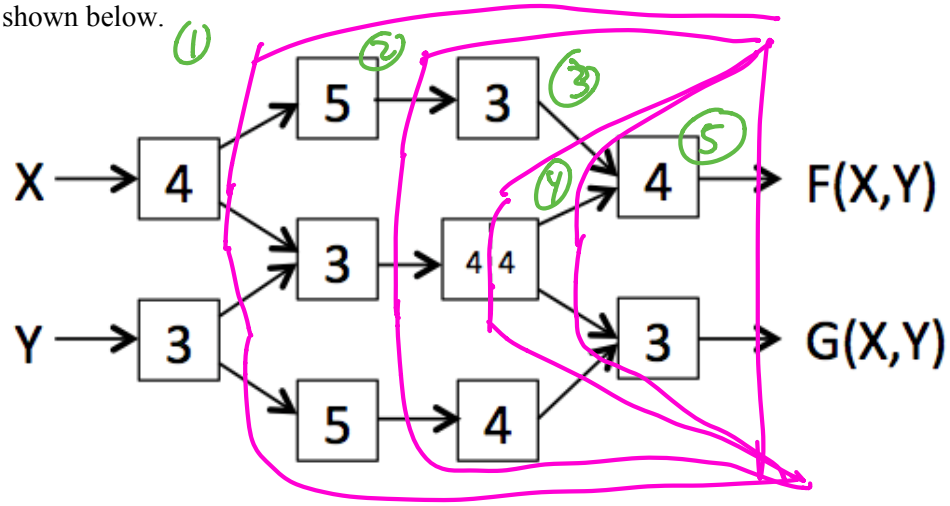



(A) Using ideal zero-delay registers, mark the location of the minimal number of registers necessary to achieve maximum throughput. Give the latency and throughput of your pipelined circuit.

**mark diagram above**

**Latency:** 3x7=21 **(ns); Throughput:** 1/7 **(1/ns)**

Rummaging through the stockroom you find a pipelined component with two pipeline stages that can replace the "7" module. The minimum $t_{CLK}$ for the new component is 4ns. The updated circuit is shown below.




(B) Using ideal zero-delay registers, mark the location of the minimal number of registers necessary to achieve maximum throughput. Give the latency and throughput of your pipelined circuit.

**mark diagram above**

**Latency:** 5x5=25 **(ns); Throughput:** 1/5 **(1/ns)**