

The Maybe Type

- Maybe#(T) represents an **optional** value of type T
 - Either Invalid and no value, or Valid and a value
- Possible implementation: A value + a valid bit

```
typedef struct { Bool valid; T value; } Maybe#(type T);  
▪ Although we could implement our own, optional values are  
so common that Maybe#(T) has a few built-in operations  
  
Maybe#(Word) x = Invalid; // no need to give value!  
Maybe#(Word) y = Valid(42); // must specify a value  
  
if (isValid(y)) // check validity  
    Word z = fromMaybe(?, y); // extract valid value
```

GCD in Minispec First version

```
typedef Bit#(32) Word;  
module GCD;  
    Reg#(Word) x(1);  
    Reg#(Word) y(0);  
    input Bool start;  
    input Word a;  
    input Word b;  
    rule gcd;  
        if (start) begin  
            x <= a; y <= b;  
        end else if (x != 0) begin  
            if (x >= y) begin // subtract  
                x <= x - y;  
            end else begin // swap  
                x <= y; y <= x;  
            end  
        end  
    endrule  
    method Word result = y;  
    method Bool isDone = (x == 0);  
endmodule
```

New GCD computation is started by setting start input to True and passing arguments through inputs a and b

Several cycles later, the module will signal it has finished through isDone. Then, the result gcd(a,b) will be available through the result method.

what if start=false? x & y never declared

if we don't check isDone, the result might be wrong

Improved GCD Module Using Maybe Types

```
typedef struct {Word a; Word b;} GCDArgs;  
module GCD;  
    Reg#(Word) x(1);  
    Reg#(Word) y(0);  
    input Maybe#(GCDArgs) in;  
    rule gcd;  
        if (isValid(in)) begin  
            let args = fromMaybe(?, in);  
            x <= args.a; y <= args.b;  
        end else if (x != 0) begin  
            if (x >= y) begin // subtract  
                x <= x - y;  
            end else begin // swap  
                x <= y; y <= x;  
            end  
        end  
    endrule  
    method Maybe#(Word) result =  
        (x == 0)? Valid(y) : Invalid;  
endmodule
```

New GCD computation is started by setting a Valid input in (which always includes a and b)

When GCD computation finishes, result becomes a Valid output

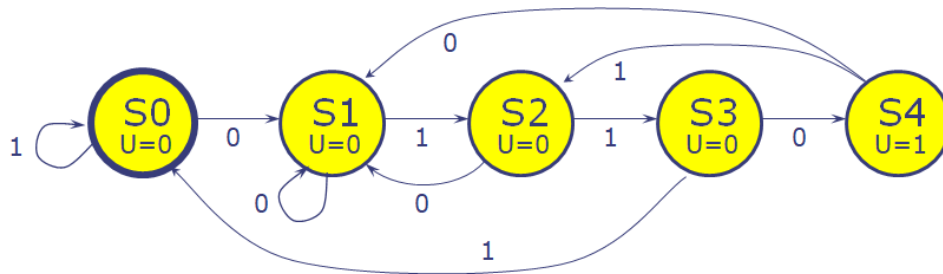
6.004 Tutorial Problems

L11 – Sequential Circuits in Minispec

Note: A subset of problems are marked with a red star (★). We especially encourage you to try these out before recitation.

Problem 1. ★

Implement the combination lock FSM from Lecture 10 as a Minispec module. The lock FSM should unlock only when the last four input bits have been 0110. The diagram below shows the FSM's state-transition diagram.



(A) Implement this state-transition diagram by filling in the code skeleton below. Use the State enum to ensure state values can only be S0-S5.

```

typedef enum { S0, S1, S2, S3, S4 } State;

module Lock;
  Reg#(State) state(S0);

  input Bit#(1) in;

  rule tick;
    state <= case (state)
      S0: (in==0)? S1: S0 _____;
      S1: (in==0)? S1: S2 _____;
      S2: (in==0)? S1: S3 _____;
      S3: (in==0)? S4: S0 _____;
      S4: (in==0)? S1: S2 _____;
    endcase;
  endrule

  method Bool unlock = (state == S4) _____;
endmodule

```

(B) How many flip-flops does this lock FSM require to encode all possible states?

5 possible states requires 3 bits to store

(C) Consider an alternative implementation of the Lock module that stores the last four input bits. Fill in the skeleton code below to complete this implementation.

```
module Lock;
  Reg#(Bit#(4)) lastFourBits(4'b1111);
  input Bit#(1) in;

  rule tick;
    lastFourBits <= { lastFourBits [2:0], in };
  endrule

  method Bool unlock = { lastFourBits == 4'b0110 };
endmodule
```

Shift left by 1, & then OR it with in

Something to remember:

MINISPEC:

rule update;

count <= count + 1;

x <= count * 4;

y <= x + 1;

endrule

previous state:

count = 3

x = 8

y = 5

PYTHON:

count = count + 1

x = count * 4

y = x + 1

count = 3 + 1 = 4

x = 4 * 4 = 16

y = 16 + 1 = 17

In minispec, registers are updated at the END of the cycle.

Problem 2. ★

Implement the Fibonacci FSM from Problem 3 of the previous worksheet by filling in the code skeleton below.

```
// Use 32-bit values
typedef Bit#(32) Word;
```

```
module Fibonacci;
  Reg#(Word) x(0);
  Reg#(Word) y(0);
  Reg#(Word) i(0);
```

```
  input Maybe#(Word) in default = Invalid;
```

```
  rule tick;
```

```
    if (isValid(in)) begin
      x <= 1;
      y <= 0;
      i <= fromMaybe(?, in) - 1;
    end else if (i > 0) begin
      x <= x + y;
      y <= x;
      i <= i - 1;
    end
```

```
  endrule
```

```
  method Maybe#(Word) result = (i == 0) ? Valid(x) : Invalid;
endmodule
```

We update x, y , and i at each clock cycle.
We check for a valid input to load into i
Result is found at x when $i = 0$

$$F_0 = 0, F_1 = 1, F_N = F_{N-1} + F_{N-2} \quad \forall N \geq 2$$

next state computation eqn:

$$i^{t+1} = i^t - 1$$

$$y^{t+1} = x^t$$

$$x^{t+1} = x^t + y^t$$

Problem 3.

Implement a sequential circuit to compute the factorial of a 16-bit number.

- (A) Design the circuit as a sequential Minispec module by filling in the skeleton code below. The circuit should start a new factorial computation when a Valid input is given. Register **x** should be initialized to the input argument, and register **f** should eventually hold the output. When the computation is finished, the result method should return a Valid result; while the computation is ongoing, result should return Invalid.

You can use the multiplication operator (*). * performs unsigned multiplication of Bit#(n) inputs. Assume inputs and results are unsigned. Though we have not yet seen how to multiply two numbers, lab 5 includes the design of a multiplier from scratch.

```
module Factorial;
  Reg#(Bit#(16)) x(0);
  Reg#(Bit#(16)) f(0);

  input Maybe#(Bit#(16)) in default = Invalid;

  rule factorialStep;

  endrule

  method Maybe#(Bit#(16)) result =
  _____;
endmodule
```

- (B) Manually synthesize your Factorial module into a sequential circuit with registers and combinational logic blocks (similar to how Lecture 11 does this with GCD). No need to draw the implementation of all basic signals (e.g., you can give formulas, like for the sel signal in Lecture 11).

Problem 4. Sequential Circuits in Minispec (Fall 2019 Quiz 2, Problem 3, 18 points)

You join a startup building hardware to mine Dogecoins. In this cryptocurrency, mining coins requires repeatedly evaluating a function with two arguments, $sc(x, y)$. x is given to you, and mining requires trying different values of y until you find a y for which $sc(x, y)$ is below a threshold value. Finding such a y value yields several Dogecoins as a reward, which you can then exchange for cold hard cash.

Because the sc function is expensive, it is implemented as a multi-cycle sequential module, called SC . SC is given to you. Its implementation is irrelevant, and its interface, shown below, is the usual interface for multi-cycle modules: SC has a single input, in , and a single method, $getResult()$. To start a new computation, the module user sets in to a `Valid Args` struct containing arguments x and y . Some cycles later, SC produces the result as a `Valid` output of its $getResult()$ method. While SC is processing an input, the $getResult()$ method returns `Invalid` and in should stay `Invalid`.

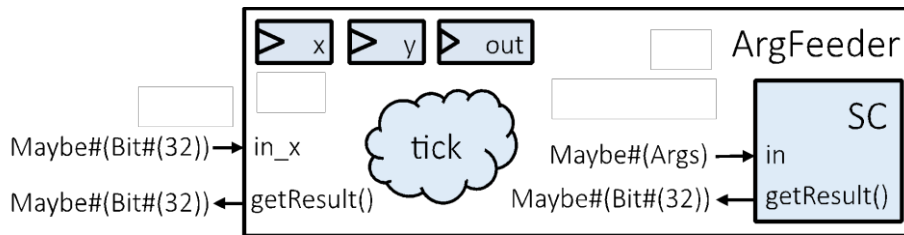
```

module SC;
    input Maybe#(Args) in default = Invalid;
    method Maybe#(Bit#(32)) getResult();
        // unknown implementation
    endmethod

    // unknown rules
endmodule

// input struct to SC
typedef struct {
    Bit#(32) x;
    Bit#(32) y;
} Args;
    
```

You are asked to design the `ArgFeeder` module, which accepts an input x , and feeds a sequence of inputs $(x, 0)$, $(x, 1)$, $(x, 2)$, ..., $(x, y-1)$, (x, y) to the SC module. `ArgFeeder` keeps feeding values to SC until SC 's result is less than **threshold** (a parameter to your module). At that point, `ArgFeeder` should return the y such that (x, y) meets this condition through its $getResult()$ method. The diagram below sketches the implementation of `ArgFeeder`. Like SC , `ArgFeeder` follows the usual interface for a multi-cycle module.



Implement the `ArgFeeder` module by completing the implementation of the `getResult()` method and the `tick` rule. The rule considers three cases:

- (i) a new input is provided to `ArgFeeder`,
- (ii) SC returns a `Valid` result, and it is *less* than the threshold value, and
- (iii) SC returns a `Valid` result, but it is *not less* than the threshold value.

You may use any Minispec operator, including arithmetic (+, -, *, /). You will not need additional registers to complete this problem. Do not add additional rules, methods, or functions.

```

module ArgFeeder#(Integer threshold);
  SC sc;

  Reg#(Maybe#(Bit#(32))) out(Invalid);
  RegU#(Bit#(32)) x;
  RegU#(Bit#(32)) y;

  input Maybe#(Bit#(32)) in_x default = Invalid;

  method Maybe#(Bit#(32)) getResult();
    // implement the getResult() method
    return  ;
  endmethod

  rule tick;
    if (isValid(in_x)) begin
      // case (i): received a new input; start a new sequence of (x, y) pairs
      sc.in = Valid(Args{x: , y: });
      out <=  ;
      x <=  ;
      y <=  ;

      end else if (isValid(sc.getResult())) begin
        if (fromMaybe(?, sc.getResult()) < threshold) begin
          // case (ii): result satisfies threshold
          out <=  ;

          end else begin
            // case (iii): result does not yet satisfy threshold
            // send next (x, y) pair to SC
            sc.in = Valid(Args{x: , y: });
            y <=  ;

          end
        end
      endrule
endmodule

```


Problem 5. Sequential Minispec (Spring 2020 Quiz 2, Problem 4, 16 points)

The incomplete Minispec module, `FindLongestBitRun`, below counts the length of the longest string of 1's in a 32-bit word. The algorithm works by repeatedly performing a bitwise AND of the word with a version of itself that has been left-shifted by one. This repeats until the word is 0. The number of iterations required is the longest string of 1's in the word. This works because each iteration converts the last 1 in any string of 1's into a 0. The word will not equal zero until its longest string of 1's has all been converted into 0's.

The circuit should start a new computation when a Valid input is given and `bitString` is 0. The `bitString` register should be initialized to the input argument, and register `n` should hold the output. When the computation is finished, the `result` method should return a Valid result; while the computation is ongoing, `result` should return Invalid.

```
typedef Bit#(32) Word;

module FindLongestBitRun;
  Reg#(Bool) initialized(False);
  Reg#(Bit#(6)) n(0);
  Reg#(Word) bitString(0);

  input Maybe#(Word) in default = Invalid;

  method Maybe#(Bit#(6)) result;
    return (initialized && bitString == 0) ?     [Part A1]     :     [Part A1]    ;
  endmethod

  rule tick;
    if (isValid(in) && bitString == 0) begin
      n <= 0;
      bitString <=     [Part A2]    ;
      initialized <= True;
    end else if (initialized && (bitString != 0)) begin
      n <= n + 1;
      bitString <=     [Part A3]    ;
    end
  endrule
endmodule
```

(A) (8 points) There are blanks in the code above labeled [Part A#]. #]. **Fill in the missing code, by copying each of the lines below and filling in the blanks corresponding to parts A1, A2, and A3.**

You may use any Minispec operators, built-in functions, and literals. You will not need additional registers to complete this problem. Do not add other rules, methods, or functions.

(Label: 4A_1) A1: `return (initialized && bitString == 0) ? _____ :`
`_____;`

(Label: 4A_2) A2: `bitString <= _____;`

(Label: 4A_3) A3: `bitString <= _____;`

(B) (8 points) At cycle 0, the input is set to Valid(32'b0111). **Copy and fill in the table below to indicate the values at the output of the result() method, the value in register n, and the value in the bitString register.** Write “Invalid” if a value is invalid, “?” if a value is unknown, and just a number to indicate a valid value (i.e. you do not need to write “Valid(5)”; just write “5”). “0b” indicates that the number after it is a binary value.

(Label: 4B) Copy and fill in the table below

Cycle	0	1	2	3	4	5	6
Input	0b0111	Invalid	0b1111	Invalid	0b0001	Invalid	Invalid
result() output							
value in register n							
value in bitString							